Chiplet Design and Heterogeneous Integration Packaging

John H Lau
Unimicron Technology Corporation

Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (either side-by-side, stacked, or both) with different sizes and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem on a common package substrate. These chips can be any kind of devices and don't have to be chiplets. On the other hand, for chiplets, they have to use the heterogeneous integration to package them. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in chiplet design and HI packaging will be presented.

Course Outline:

1. Introduction
2. System-on-Chip (SoC)
3. Chiplet Design and HI Packaging
4. Advantages and Disadvantages of Chiplet Design and HI Packaging
5. AMD Chiplet Design and HI Packaging: (a) EPYZ and (b) RYZEN
6. Intel Chiplet Design and HI Packaging: (a) FOVEROS, (b) FOVEROS Direct, and (c) Ponte Vecchio
7. TSMC chiplet Design and HI Packaging: (a) SoIC, (b) SoIC + CoWoS, and (c) SoIC + InFO PoP
8. Chiplets Lateral Interconnects (Bridges): (a) Intel's EMIB, (b) IBM's solution for EMIB, (c) Applied Materials' Bridge Embedded in Fan-Out EMC, (d) SPIL's FO-EB, (e) TSMC's LSI, (f) ASE's sFOCoS, (g) IME's EFI, and (h) Amkor's S-Connect Fan-Out Interposer
9. HI Packaging on Organic Substrates: many examples
10. HI Packaging on Silicon Substrates (TSV-Interposers): many examples: (a) Leti, (b) IME, (c) HKUST, (d) ITRI, (e) Xilinx/TSMC, (f) Altera/TSMC, (g) NVidia/TSMC, (h) AMD/UMC, (i) AMD's Active Interposer, (j) Intel's FOVEROS, (k) TSMC's SoIC, and (l) Samsung's X-Cube
11. HI Packaging on Silicon Substrates (TSV-Less Interposers) such as Bridges: Same as 8
12. HI Packaging on Ceramic Substrate: one example
13. HI Packaging on Fan-Out RDL for High Performance Applications: many examples: (a) STATSChipPac's FOFC-eWLB, (b) ASE's FOCoS, (c) MediaTek's FO-RDLs, (d) TSMC's InFO_oS and InFO_MS, (e) Samsung's Si-Less RDL Interposer, (f) TSMC's RDL-Interposer, (g) ASE's FOCoS (Chip-Last), (h) Shinko's Organic RDL-Interposer, and (i) Unimicron's Hybrid Substrate
14. Assembly Technologies for Chiplet Design and HI Packaging: (a) SMT, (b) Solder Bumped Flip Chip, (c) CoW, (d) WoW, (e) TCB, and (f) Bumpless Cu-Cu Hybrid Bonding
15. Trends in Chiplet Design and HI Packaging

Who Should Attend?

If you (students, engineers, and managers) are involved with any aspect of the electronics industry, you should attend this course. It is equally suited for R&D professionals and scientists. The lectures are based on the publications by many distinguish authors and the books (by the lecturer) such as *Heterogeneous Integration* (Springer, 2019) and *Semiconductor Advanced Packaging* (Springer, 2021). Each attendee will receive more than 150 pages of lecture notes.

Lecturer Bio

John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging and SMT assembly, has published more than 500 peer-reviewed papers, 30 issued and pending US patents, and 22 textbooks on, e.g., *Reliability of RoHS compliant 2D & 3D IC Interconnects* (McGraw-Hill, 2011), *Through-Silicon Via (TSV) for 3D Integration* (McGraw-Hill, 2013), *3D IC Integration and Packaging* (McGraw-Hill, 2016), *Fan-Out Wafer-Level Packaging* (Springer, 2018), and *Assembly and Reliability of Lead-Free Solder Joints* (Springer, 2020), John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow.