

# Trends in Analog and Power Packaging

Dan Kinzer

Fairchild Semiconductor Corp., 3001 Orchard Parkway, San Jose, Ca., 95134, USA

## ABSTRACT:

The technology in packaging of electronic components continues to advance at an impressive pace. As the analog and power chips get smaller, the importance of the package increases more and more. The package can be a substantial portion of the cost of the component, and controls many of the key electrical parameters and much of the reliability performance of the end product. It defines the form of the final product, drives miniaturization and heat transfer, and forms the mechanical and electrical connections to the rest of the system. There are many new technologies in packaging. In this paper, the intent is to focus on a few of those as they impact single component packaging and multichip packaging combining power and analog into a more complex power function. There will also be some products that have a hierarchy of levels of packaging, in which a system level package contains packaged components inside.

Analog products range in pin count from 3 leaded devices to several dozens of leads or more for very complex functions. For most of these, the drive has been to reduce the form factor to keep pace with the shrinking IC. The industry has moved from DIP to SOP to SSOP to TSSOP to MLP. With MLP, there are different variations depending on whether there is an exposed DAP or not. Further, the pitch of the MLP continues to shrink, dropping down to .5mm, .4mm, and .35mm, with further shrinks to come. For higher pin counts, single row MLP is not enough to continue reducing the form factor, leading to dual row MLP, and eventually to array packages like the BGA and the wafer level CSP. These array packages are also following similar trends in pitch reduction. Further, to enable the BGA to shrink down to near the size of the die, the Flip Chip BGA is gaining in importance. Once that technology is in place, the door is open to a host of other forms of stacked die packaging, package on package, and other more complex advanced approaches. Meanwhile the customers continue to seek thinner solutions, moving the bar from .75mm to .55mm to .4mm and less. This can drive a move away from the conventional solder ball approach to more of a bumped or thin plated land pattern. It also forces the use of thin substrates or leadframes, and interconnection systems that do not have the loop height requirements of conventional wirebonding.

The basic building block of most power systems is the power transistor, usually a MOSFET or an IGBT. Power MOSFETs have also been shrinking at a rapid pace, especially in the voltage range of 40V and below. As the chips shrink 10-15% annually, the packaging imperative is to lower the package parasitic resistance and inductance, as well as to provide a high thermal conductivity to remove the heat. Lately MLP packages, known in some cases as Power QFNs, have been gaining a great deal of

popularity due to their small form factor, exposed DAP for lower thermal resistance to the PCB, and solid reliability. Internal connections until recently were predominantly gold wire bonding, but that has been giving way to copper bonding, thick aluminum wire and ribbon bonding, and clip bonding. These interconnection methods are compared in thermal, electrical, and mechanical performance. In addition, the added feature of top sided cooling will be discussed for higher power applications that will use forced air cooling and top side heatsinks. This will be discussed in the case of the Power56, which has the popular 5X6mm footprint, but similar approaches can be applied to the smaller Power33, and even smaller in the future. Another important trend for low voltage power MOSFETs is the use of dual die packaging. In particular, a class of devices with optimized high side and low side combinations for specific DC-DC applications is available in 3X3mm and 5X6mm sizes. Where less power is needed, the WLCSP MOSFET is an excellent alternative. This MOSFET is available in 1X1.5mm 6-ball versions, with thickness down to .4mm, and also in a 1X1 4-ball version. Since a 10 milliohm MOSFET can now be fabricated in about that size, these devices will be able to handle sizable currents up to 5A or more.

Power circuits that use analog drivers and controllers combined with power devices are often combined in multichip assemblies. In a DrMOS device, the driver IC combines with two FETs to deliver a complete power stage function. The new 6X6mm DrMOS devices can deliver over 30A in a footprint dramatically smaller than three individually packaged units and a significant reduction over the more conventional 8X8mm. In addition, the tight coupling and mutual optimization of the chips can provide better consistency and converter efficiency than a discrete design. When a controller is co-packaged, as in the Tinybuck™, a medium power closed loop complete semiconductor solution is the result. In some cases, it is advantageous to include prepackaged passive elements such as capacitors and inductors as well. These can be combined in a package either on PCB or tape interposer substrates or on leadframe based assemblies. For higher power systems like motor drive inverters, complicated co-packaged assemblies with multiple drive and control ICs and up to 12 power devices are available. These are designed for optimal thermal performance using ceramic, direct bond copper (DBC), or insulated metal substrates (IMS).

This paper will provide examples of implementations of these packaging technologies, the simulation methods that have been used to design them, and project the future trends.